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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/399,510
Filing Date: September 20, 1999
Appellant(s): DONG ET AL.

Chun M. Ng
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 29 September 2004.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

The rejection of Claims 1 – 3, 6, 7, and 10 stand or fall together because Appellant's brief does not include a statement that this grouping of claims does not stand or fall together and reasons in support thereof. See 37 CFR 1.192(c)(7).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

6,597,395 B1	KIM et al.	07-2003

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. **Claims 1, 2, 6, 7, and 10** are rejected under 35 U.S.C. 102(e) as being anticipated by Kim et al.

3. For **Claim 1**, Kim et al. disclose, as shown in figure 2 and as stated in columns 3 (lines 7 – 67), 4 (lines 1 – 10), and 5 (lines 1 – 26), a method for auto black expansion in an image sensor (CCD 100), comprising:

(a) comparing (performed in the Digital Comparator – 230) the voltage level of processed pixel signals (CDS/AGC – 200 process the signals by performing correlated double sampling) with a first set voltage level (voltage level B from the microcomputer);

(b) maintaining a first count of a number of pixels signals that are above or below the first set voltage level (Up/Down Counter – 240 raises and or lowers a running count depending

upon whether the pixels signals are greater than or less than the first set voltage level; see column 3, lines 65 – 67, and column 4, lines 1 – 4); and

(c) using the count to determine a first digital control signal for adjusting the black level calibration of the processed pixel signals (The Up/Down Counter – 240 and the Digital Comparator – 230 both accept and output digital signals. An n-bit control signal, provided by the Up/Down Counter – 240, is applied to the D/A Converter – 250 so as to provide control for a Black Level Clamp Circuit – 260. The n-bit digital control signal, provided by the Up/Down Converter – 240, is required for adjusting the black level calibration.); and

(d) comparing (Black Level Clamp Circuit 260) the pixel signals to a second set voltage level (The second set voltage level is the "divided" voltage value selected from a plurality of divided voltages by the D/A Converter – 250, according to the control signal; see column 3, lines 25 – 27, column 4, line 63 – 68, and column 5, lines 1 – 4) different from said first set voltage level (as will become evident in the explanations below) and maintaining a second count related to the comparison of the pixel signals to the second level (see explanation below), wherein the second count (provided by Up/Down Counter – 240 dependent upon the new processed pixel signals) is used to determine a second digital control signal for adjusting the amplification of the processed pixel signals.

The whole object of Kim et al. is to establish two different lower phase reference voltages. One lower phase reference voltage (V_B), generated by the reference voltage generator (220), is applied to the A/D Converter (210). The other of the two different lower phase reference voltages (not labeled but clearly shown in figure 2) is established by the D/A Converter (250) and is identified, in figure 2, as the signal output from the D/A Converter (250) and input

into the Black Level Clamp Circuit (260). The D/A Converter (250) accepts two inputs: the n-bit control signal output from the Up/Down Counter (240) and the one lower phase reference voltage (V_B). The D/A Converter (250) divides the one lower phase reference voltage (V_B), according to the n-bit control signal, into the other of the two different lower phase reference voltages (not labeled but clearly shown in figure 2).

Regarding the claim language, the processed pixel signals (output from CDS/AGC – 200) are compared in the Black Level Clamp Circuit (260) to the "divided" voltage value output from the D/A Converter (250). The same processed pixel signals (i.e. the processed pixel signals are output from the CDS/AGC – 200) are compared to a first set voltage level (voltage level B) in the Digital Comparator (230) and then are compared to a second set voltage level ("divided" voltage value) in the Black Level Clamp Circuit (260). Because, Kim et al. disclose a feedback loop to effect Black Level Calibration, a first count is maintained by the Up/Down Counter (240) prior to the generation of the n-bit control signal and a second count is maintained by the Up/Counter Down Counter (240) after generation of the n-bit control signal and comparison to the second set voltage level. In other words, the first count is used to generate the n-bit control signal so as to generate the second set voltage level. The Black Level Clamp Circuit (260) clamps the black level in the processed pixel signals to the second set voltage level. The resultant clamped signal is fed back to the CDS/AGC (200) to become new processed pixel signals. The new processed pixel signals are compared in the Digital Comparator (230) so as to establish a second count relating to the comparison of the processed pixel signals to the second level. Since, the new processed pixel signals are dependent upon the comparison in the Black Level Clamp Circuit (260) to the second set voltage level, the second count using the new

processed pixel signals in the Up/Down Counter (240) is "related to the comparison," (as claimed). The Up/Down Counter (240) and the Digital Comparator (230) both accept and output digital signals. An n-bit control signal, provided by the Up/Down Counter (240), is applied to the D/A Converter (250) so as to provide control for a Black Level Clamp Circuit (260), which in turn further provides control to the amplifier circuit (CDS/AGC Circuit – 200). The n-bit digital control signal, provided by the Up/Down Converter – 240, is required for adjusting the black level calibration and amplifying the pixel signals.

4. As for **Claim 2**, Kim et al. disclose the method Claim 1, wherein the adjustments to the black level calibration are made in between fields of pixels signals.

The Applicant defines, on pages 2 (lines 16), 3 (lines 15 and 16), 4 (line 3), 8 (line 18), 9 (lines 16 and 17), 10 (lines 21 and 22), and 12(line 1), that a "field of pixel signals" corresponds to an image signal, or rather a "sensed image" or a "scene". Thus, Kim et al. teach that adjustments to the black level calibration are made on image signals, as stated in column 3 (lines 14 – 18), and thus, are made between fields of pixel signals.

5. As for **Claim 6**, Kim et al. disclose, as shown in figure 2, the method of Claim 5, wherein adjustments to the amplification (CDS/AGC Circuit – 200) of the processed pixel signals are only made after adjustments to the black level calibration (Black Level Clamp Circuit – 260) have adjusted the pixel signals to a desired voltage level.

The black level of the pixels signals is adjusted prior to amplification. In other words, it is necessary to adjust the black level of the pixels prior to adjusting the amplification of the pixel signals.

6. For **Claim 7**, Kim et al. disclose, as shown in figure 2 and as stated in columns 3 (lines 7 – 67), 4 (lines 1 – 10), and 5 (lines 1 – 26), an image sensor (CCD 100) for processing image signals that are comprised of processed pixel signals, the image sensor comprising:

(a) auto black expansion circuitry for adjusting the relative voltage level of the image signal (The Digital Comparator – 230, Up/Down Counter – 240, D/A Converter – 250, Black Level Clamp Circuit – 260, and CDS/AGC Circuit – 200 are all required for adjusting the black level calibration of the image signals);

(b) a black level voltage input (Black Level Calibration Voltage B, first iteration of the feedback loop);

(c) a comparator (Digital Comparator – 230, first iteration of the feedback loop), the comparator comparing the processed pixel signals (Image Signal A) to the desired black level signal (Black Level Calibration Voltage B, first iteration of the feedback loop);

(d) a counter (Up/Down Counter – 240) for maintaining a count related to the comparison performed by the comparator (Up/Down Counter – 240 raises and or lowers a running count depending upon whether the image signal is greater than or less than the Black Level Calibration Voltage B, first iteration of the feedback loop; see column 3, lines 65 – 67, and column 4, lines 1 – 4); and

(e) a digital controller (D/A Converter – 250) for utilizing the count maintained by the counter to determine desired adjustments to the auto black expansion circuitry (The Up/Down Counter – 240 and the Digital Comparator – 230 both accept and output digital signals. An n-bit control signal, provided by the Up/Down Counter – 240, is applied to the D/A Converter – 250 so as to provide control for a Black Level Clamp Circuit – 260. The n-bit digital control signal,

provided by the Up/Down Converter – 240, is required for adjusting the black level calibration), and

(f) a mid-level voltage input (The mid-level voltage input is the "divided" voltage value selected from a plurality of divided voltages by the D/A Converter – 250, according to the control signal; see column 3, lines 25 – 27, column 4, line 63 – 68, and column 5, lines 1 – 4) different from said black level voltage input (as will become evident in the explanations below) and a second comparator (Black Level Clamp Circuit 260) for comparing processed pixel signals to the mid-level voltage input (see explanation below); and

(g) automatic gain control circuitry (200), wherein the digital controller (250) utilizes the count of a second counter to determine adjustments to the automatic gain control circuitry (200).

The whole object of Kim et al. is to establish two different lower phase reference voltages. One lower phase reference voltage (V_B), generated by the reference voltage generator (220), is applied to the A/D Converter (210). The other of the two different lower phase reference voltages (not labeled but clearly shown in figure 2) is established by the D/A Converter (250) and is identified, in figure 2, as the signal output from the D/A Converter (250) and input into the Black Level Clamp Circuit (260). The D/A Converter (250) accepts two inputs: the n-bit control signal output from the Up/Down Counter (240) and the one lower phase reference voltage (V_B). The D/A Converter (250) divides the one lower phase reference voltage (V_B), according to the n-bit control signal, into the other of the two different lower phase reference voltages (not labeled but clearly shown in figure 2).

Regarding the claim language, the processed pixel signals (output from CDS/AGC – 200) are compared in the Black Level Clamp Circuit (260) to the "divided" voltage value output from

the D/A Converter (250). The same processed pixel signals (i.e. the processed pixel signals are output from the CDS/AGC – 200) are compared to a black level voltage input (voltage level B) in the Digital Comparator (230) and then are compared to a mid-level voltage input ("divided" voltage value) in the Black Level Clamp Circuit (260). Because, Kim et al. disclose a feedback loop to effect Black Level Calibration, a first count is maintained by the Up/Down Counter (240) prior to the generation of the n-bit control signal and a second count is maintained by the Up/Counter Down Counter (240) after generation of the n-bit control signal and comparison to the mid-level voltage input. In other words, the first count is used to generate the n-bit control signal so as to generate the mid-level voltage input. The Black Level Clamp Circuit (260) clamps the black level in the processed pixel signals to the mid-level voltage input. The resultant clamped signal is fed back to the CDS/AGC (200) to become new processed pixel signals. The new processed pixel signals are compared in the Digital Comparator (230) so as to establish a second count relating to the comparison of the processed pixel signals to the mid-level voltage input. Since, the new processed pixel signals are dependent upon the comparison in the Black Level Clamp Circuit (260) to the mid-level voltage input, the second count using the new processed pixel signals in the Up/Down Counter (240) is related to the comparison. The Up/Down Counter (240) and the Digital Comparator (230) both accept and output digital signals. An n-bit control signal, provided by the Up/Down Counter (240), is applied to the D/A Converter (250) so as to provide control for a Black Level Clamp Circuit (260), which in turn further provides control to the amplifier circuit (CDS/AGC Circuit – 200). The n-bit digital control signal, provided by the Up/Down Converter – 240, is required for adjusting the black level calibration and amplifying the image signal.

7. As for **Claim 10** (see objection above), Kim et al., disclose, the image sensor of Claim 7, wherein the adjustments to the auto black expansion circuitry are made in between field of pixel signals.

The Applicant defines, on pages 2 (lines 16), 3 (lines 15 and 16), 4 (line 3), 8 (line 18), 9 (lines 16 and 17), 10 (lines 21 and 22), and 12(line 1), that a "field of pixel signals" corresponds to an image signal, or rather a "sensed image" or a "scene". Thus, Kim et al. teach that adjustments to the black level calibration are made on image signals, as stated in column 3 (lines 14 – 18), and thus, are made between fields of pixel signals.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. **Claim 3** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al.

10. As for **Claim 3**, Kim et al. disclose, the method of Claim 1, wherein the digital control signal comprises n-bits.

Kim et al. teach that the control signal is an n-bit digital control signal, as stated in column 4 (line 9). Kim et al. in no way limit the number of bits included in the digital control signal, and hence, Kim et al. do not specifically disclose an 8-bit digital control signal. However, an 8-bit control signal is commonly known and used in the art and, thus, at the time

the invention was made one with ordinary skill in the art would have been motivated to and it would have been obvious for Kim et al. to have used an 8-bit control signal.

(11) Response to Argument

11. **In response to the summary of Kim et al. as presented by Appellant,** the Examiner is aware and acknowledges that Kim et al. does not work the same or have the same elements of the apparatus of figure 3 and the corresponding method of figures 5A – 5C of the present invention. Nonetheless, the Examiner believes that, in the very least, Claims 1 and 7 are written broadly enough such that each and every limitation therein is anticipated by Kim et al. under 35 U.S.C. 102(e).

12. Kim et al. provides a black level calibration apparatus for a video camera, wherein a present black level A and a black level calibration value B are continuously compared, by means of a feedback loop, until the two values are determined to be identical. Turning to figure 2, Kim et al. operates according to the following:

13. Initially, an output signal from a Charge Coupled Device (CCD) image sensor and a feedback signal from the Black Level Clamp Circuit 260 (to be described later) is input into a Correlated Double Sampling/Automatic Gain Control (CDS/AGC) circuit 200, wherein based upon the feedback signal, sample-and-hold and automatic gain control processing is applied to the image sensor input signal, thereby yielding a processed image signal. The processed image signal is then applied to an input of the Black Level Clamp Circuit 260 (to be described later) and to the analog-to-digital (A/D) converter 210, wherein in the A/D converter 210, the

processed image signal is converted into a processed digital image signal. The processed digital image signal is then applied to input A of the Digital Comparator 230, wherein the black level of the processed digital image signal is compared with a predetermined black level calibration value B, received from a microcomputer, and a compared resultant value is accordingly output. The digital compared resultant value output from the Digital Comparator 230 is applied to the Up/Down Counter 240, wherein the Up/Down Counter 240 raises or lowers a present count value in accordance with the resultant value; thereby outputting an n-bit digital control signal to be applied to the digital-to-analog (D/A) converter 250. In accordance with the input n-bit digital control signal, the D/A converter 250 outputs a voltage value selected from a plurality of divided voltage values, wherein the selected voltage value is then input into the Black Level Clamp Circuit 260. As described above, the Black Level Clamp Circuit 260 is input with the processed image signal (provided from CDS/AGC circuit 200) and is input with the selected voltage value (provided from D/A converter 250), wherein the Black Level Clamp Circuit 260 clamps the processed image signal in accordance with the selected voltage value. The clamped processed image signal is fed back to the CDS/AGC circuit 200; thereby completing the feedback loop. This process is repeated until the black level of the processed digital image signal is identical to the predetermined black level calibration value.

14. For the purposes of interpretation and understanding, each iteration of the feedback loop starting and ending with the CDS/AGC circuit 200 will be assigned to a respective time instant; wherein a first iteration, as described above, takes place during time instant 1 (herein referred to **T1**) and wherein a second iteration takes place, after the first iteration and dependent upon the results of the first iteration (as indicated by the clamped processed image signal being fed-back

into the CDS/AGC circuit 200), during time instant 2 (herein referred to **T2**). Furthermore, in accordance with the Examiner's rejection of Claim 1 as detailed above, limitations (a), (b), (c), and the "comparing the pixel signals to a second set voltage level different from said first set voltage level an" portion of (d) are fully encompassed by the operation of Kim et al. during T1. Furthermore, in accordance with the Examiner's rejection of Claim 1 as detailed above, the remaining portion of limitation (d), beginning and ending with "and maintaining a second count ... for adjusting the amplification of the processed pixels signals," respectively, is fully encompassed by the operation of Kim et al. during T2. The same thought can equally be applied to Claim 7, as will become evident below.

15. Turning to Claim 1, the claim language is anticipated by Kim et al. as follows:

A method for auto black expansion in an image sensor, comprising:

(a) comparing the voltage level of processed pixel signals (output from CDS/AGC 200 **@ T1**) with a first set voltage level (Black Level Calibration Value B **@ T1**),

(b) maintaining a first count of a number of pixel signals (Within Up/Down Counter 240 **@ T1**) that are above or below the first set voltage level;

(c) using the count to determine a first digital control signal (n-bit digital control signal output from Up/Down Counter 240 **@ T1**) for adjusting the black level calibration of the processed pixel signals, and

(d) comparing the pixel signals to a second set voltage level ("Divided voltage value" selected from a plurality of voltage values in D/A Converter 250 **@ T1**) different from said first set voltage level and maintaining a second count (Within Up/Down Counter 240 **@ T2**) related to the comparison of the pixel signals to the second level, wherein the second count is used to

determine a second digital control signal (n-bit digital control signal output from Up/Down Counter 240 @ **T2**) for adjusting the amplification of the processed pixel signals.

16. **In response to the arguments against Kim et al. as presented by Appellant,** the Examiner respectfully disagrees as will become evident below.

17. In a first argument, the Appellant states, "the Kim patent does not teach the comparison of an individual pixel of an image to a threshold level. In contrast, the Kim patent compares an entire digital image to a voltage reference." The Appellant cites the following Claim 1 limitation: "comparing the voltage level of processed pixel signals with a first set voltage level." Initially, the Examiner would like to point out that "the comparison of an individual pixel" is not claimed. Furthermore, if the cited claim limitation were interpreted so as to require the comparison of an individual pixel with a first set voltage level, Kim et al. meets this limitation because an image frame as a whole or an entire digital image is comprised of a plurality of individual processed pixel signals. Thus, since the phrase "processed pixel signals" is extremely broad in the fact that processed pixel signals is not limited to individual pixel signals, not limited to a single image frame or entire digital image, and not limited to a plurality of image frames or entire digital image data, comparing the image frame as a whole or entire digital image fully encompasses comparing the processed pixel signals.

18. In a second argument, the Appellant states, "there is no indication that the automatic gain control block 200 can be adjusted in any manner, let alone be adjusted based upon the use of a second counter as is required in Claims 1 and 7." As stated above, a first count is maintained within Up/Down Counter 240 @ **T1** and a second count is maintained within Up/Down Counter

240 @ T2. Since the Up/Down Counter 240 maintains a first count and a second count at T1 and T2, respectively, just as at T1, the second count at T2, is used to determine the second digital control signal that input into the Black Level Clamp Circuit 260, wherein the Clamp Circuit 260 clamps the processed image signal and feeds the clamped image signal back into the CDS/AGC circuit 200.

19. In a third argument, the Appellant states, "the Kim patent does not address the modification of the automatic gain control using a **comparison to a second set voltage level independent and not based on the first set voltage level.**" The bolded phrase is not claimed in either Claim 1 or Claim 7. Even more specifically, "independent and not based on" is not stated in the claim language.

20. In a fourth argument, the Appellant states, "they are not two different unrelated voltage levels as required by the claims, but rather different versions of the same voltage level and related to each other." Initially, while "different" is claimed, the further limiting "unrelated" is not claimed. Additionally, the Appellant is vague and unclear as to which "voltage levels" are being referred to when "they" is stated; however, for the sake of argument, the Examiner will assume that the Appellant is referring to the first set voltage level and the second set voltage level. As stated above, the processed digital image signal is then applied to input A of the Digital Comparator 230, wherein the black level of the processed digital image signal is compared with a predetermined black level calibration value B, received from a microcomputer, and a compared resultant value is accordingly output to the Up/Down Counter 240. Furthermore, as stated above, in accordance with the input n-bit digital control signal, the D/A converter 250 outputs a voltage value selected from a plurality of divided voltage values,

wherein the selected voltage value is then input into the Black Level Clamp Circuit 260. As clearly defined above, the first set voltage level is the predetermined black level calibration value B and the second set voltage level is the "divided voltage value." Thus, according to Appellant's logic, the "divided voltage value" is just the analog version of the predetermined black level calibration value B, which is inaccurate. The "divided voltage value" is selected from a plurality of voltage values based upon the n-bit digital control signal which is based upon a count provided by the Up-Down counter 240, which raises or lowers a present count based upon the comparison of the digital processed image signals to the predetermined black level calibration value B. The Examiner believes the Appellant's fourth argument and remaining arguments (as will become evident below) indicate the Appellant's misunderstanding of how the Examiner is interpreting the claims.

21. In a fifth argument, the Appellant argues, "the n-bit control word is the digital version of the analog voltage output by the D/A converter 250 ... to argue Kim teaches two voltages levels and two counters is inappropriate and contrary to the a plain reading of the Kim patent." Again, Appellant's arguments indicate Appellant's misunderstanding of how the Examiner is interpreting the claims. The Up/Down Counter 240 maintains a first count at T1 and maintains a second count at T2, respectively.

22. In a sixth and final argument, the Appellant argues, "the black level clamp circuit 260 only clamps the black level of the CDS/AGC circuit 200. Thus, the black level clamp circuit 260, while providing feedback to the CDS/AGC circuit 200, does not vary the automatic gain control of the CDS/AGC circuit 200." Kim et al. specifically states, the CDS/AGC circuit 200 "performs sample/hold and automatic gain control operations on an analog image signal based

on the black level clamping signals." The black level clamping signals are the clamped processed image signals output from the Black Level Clamp Circuit 260.

23. **For the above reasons, it is believed that the rejections should be sustained.**

Respectfully submitted,

Justin P. Misleh
November 26, 2004

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